REMARKS

Applicants appreciate the examination of the present application that is set forth in the Official Action of March 1, 2004. In response to the Official Action, Applicants have amended page 1 of the specification to include the serial number of the related application and have added new Claims 65-68. Claim 30 has also been amended to better highlight how the three terminals of the PMOS transistor are connected within the match line precharge support circuit. Minor technical amendments have also been made to dependent Claim 34.

Thus, the sole outstanding issue is the rejection of Claims 30-34 based on U.S. Patent Publ. No. 2003/0123269 A1 to Gillingham et al. Applicants will now show that Claims 30-34 and the new Claims 65-68 are patentable over Gillingham et al.

Claims 30-34 and 65-68 are Patentable Over Gillingham et al.

The claims of the present application read on a portion of the CAM array illustrated by at least FIG. 6C-2 of the present application. In FIG. 6C-2, an inverter I11 is illustrated as having an input connected to a first match line segment (ML0_b) and an output that is fed back to a gate of a first PMOS pull-up transistor (P71). This first PMOS pull-up transistor P71 has a drain terminal that is connected to the first match line segment ML0_b. A second normally-on PMOS pull-up transistor (P70) is also provided to enable precharging of the first match line segment ML0_b when an output of the inverter I11 is switched high-to-low and the first PMOS transistor P71 is turned on. However, as the first match line segment ML0_b is pulled high-to-low during a lookup operation to thereby indicate a miss condition in the illustrated row of CAM cells, the output of inverter I11 is switched low-to-high and the first PMOS transistor P71 is turned off. This precludes the match line precharge support circuit from competing with the CAM cells when a miss condition is present during a lookup operation.

Independent Claim 30 of the present application recites features that support this feedback relationship whereby the output of the inverter I11 influences the precharging of the match line that is connected to an input of the inverter. For

example, independent Claim 30, which has been annotated to highlight elements shown in FIG. 6C-2, recites:

> 30. A content addressable memory (CAM) array, comprising:
> a first match line segment (**ML0_b**) associated with a first row of CAM cells in the CAM array;
> an inverter (**I11**) having an input electrically coupled to said first match line segment (**ML0_b**); and
> a match line precharge support circuit electrically connected to said first match line segment (**ML0_b**) and comprising a first PMOS transistor (**P71**), said first PMOS transistor (**P71**) having a gate terminal electrically coupled to an output of said inverter (**I11**), a first current carrying terminal (**e.g., drain terminal**) that is electrically coupled to said first match line segment (**ML0_b**) and a second current carrying terminal (**e.g., source terminal**) that is electrically coupled to a power supply line (**Vdd**).

In the embodiment illustrated by FIG. 6C-2 of the present application, the source terminal of PMOS transistor P71 is electrically coupled to the power supply line (Vdd) by the normally-on PMOS transistor P70, which operates as a voltage-controlled resistor. When the PMOS transistor P71 is turned on, the first match line segment ML0_b, which is provided to an input of the inverter I11, is pulled to (or held at) a high level.

In stark contrast, FIG. 2(a) of Gillingham et al. merely shows a plurality of match line segments MLS_0, MLS_1, ..., that are electrically coupled together by respective match line strap circuits **212**. In particular, the match line segment MLS_0 in FIG. 2(a) is shown as driving an inverter **210**. The output of the inverter **210** is connected to an input of a controlled inverter **214** that includes: a PMOS pull-up transistor and an NMOS pull-down transistor, an NMOS transistor **218**, which is responsive to a match line segment enabling signal MATLO1, and a current source **216**. However, this controlled inverter **214** does not provide any feedback of any signal to any device that controls precharging of the match line

segment MLS_0. Moreover, the PMOS pull-up transistor within the controlled inverter **214** does not have any current carrying terminal that is electrically coupled back to the first match line segment MLS_0. Thus, it cannot be reasonably maintained that Gillingham et al. discloses or suggests the subject matter of Claim 30. The dependent Claims 31-34 and new Claims 65-68 also recite aspects of the present invention that are not disclosed or suggested by the cited prior art.

Accordingly, Applicants submit that the present application is in condition for allowance, which is respectfully requested. The Examiner is encouraged to contact the undersigned in the event any issues remain which may prevent issuance of the present application.

Respectfully submitted,

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on March 18, 2004.

Candi L. Riggs
Date of Signature: March 18, 2004

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